

### **REMARKS**

The present response amends claims 1, 6, 10, 15, 16, and 20 in conformity with the following remarks. In addition, claims 7, 14, and 22 are canceled without prejudice or disclaimer as to the subject matter recited therein. Claims 1-6, 8-13, 15-21, and 23-25 remain pending in the captioned case. Further examination and reconsideration of the presently claimed application are respectfully requested.

### **Allowable Subject Matter**

Claims 6, 7, and 18 were deemed to contain allowable subject matter. In order to expedite prosecution, the limitations of claim 7 have been incorporated into independent claim 1. Accordingly, it is believed that claim 1 and claims dependent therefrom are in condition for allowance. In addition, it is believed that amendments made herein also render independent claims 10 and 20, as well as claims dependent therefrom, allowable over the art of record.

### **Section 102 Rejection**

Claims 1, 3-5, 20, 21, and 23-25 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,097,449 to Cuevas (hereinafter "Cuevas"). In light of amendments to claim 1 which incorporate the allowable subject matter from claim 7, it is believed that the rejection of claim 1 and claims dependent therefrom (claims 3-5) has been obviated. The remaining rejection of claims 20, 21, and 23-25 is hereby traversed.

The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art of reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); MPEP 2131. Furthermore, anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, as arranged in the claim. *W.L. Gore & Assocs. V. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983). Using these standards, Applicants submit the cited art fails to disclose each and every element of the currently pending claims, some distinctive features of which are set forth in more detail below.

Cuevas does not teach or suggest placing a voltage value from a data bus onto the gate of a selecting transistor during times when a source-to-drain path of a programming transistor is activated. Present claim 20 has been amended to contain the limitations from claim 22. In particular, amended claim 20 describes forwarding a latched voltage value onto a gate of a selecting transistor during times when a source-to-drain path of a programming transistor is activated. The programming transistor is activated via a programming voltage placed on a gate of the programming transistor. As shown in Fig. 5 of the present specification, the selecting transistor is shown as reference 68a/68b. The programming transistor is shown as reference 70a/70b. The voltage value from latch 12 at node 84a/84b is forwarded onto the gate of selecting transistor 68 when the source-to-drain path of programming transistor 70 is activated.

Contrary to present independent claim 20, Cuevas does not describe, illustrate, or suggest any source-to-drain path placed between the latched data bus D/D-bar and the gate of the alleged selecting transistor 51/53 (Cuevas -- Fig. 1). The fact is admitted on page 10 of the Office Action. However, the Office Action suggests that U.S. Patent No. 6,141,247 to Roohparvar et al. (hereinafter "Roohparvar") provides the nexus. Applicants respectfully disagree. Roohparvar shows only a source-to-drain path of a transistors 24/26 that is activated by a connect signal C<sub>N</sub>. First, the connect signal is not a programming voltage as alleged in the Office Action. Second and more importantly, nowhere in Roohparvar is there any mention that the source-to-drain path of transistors 24/26 connects the output from latch 12 to a gate of a pair of selecting transistors (Roohparvar -- Fig. 1). In fact, Roohparvar only suggests that the connecting transistors 24/26 connect the output from latch 12 to a drain of transistors C/C-bar (Roohparvar -- Fig. 1).

If the allegation will be made that the present claim 20 is obvious in light of a combination of Cuevas and Roohparvar, then Applicants respectfully suggest that the mere fact that Cuevas and Roohparvar can be combined or modified does not render the resulting combination obvious unless the prior art suggested the desirability of that combination. See, MPEP 2143.01; *In re Mills* 916 F.2d 680 (Fed. Cir. 1990). Specifically, there must be some suggestion or motivation in either Cuevas or Roohparvar for providing a source-to-drain path between the output of a latch and a selecting transistor. If there is no such suggestion or motivation in those references, then a *prima facie* case of obviousness cannot be established. *In re Fritch*, 972 F.2d 1260 (Fed. Cir. 1992). Certainly a skilled artisan looking at Cuevas and finding no source-to-drain path to a gate of a selecting transistor would not assume that the missing source-to-drain path can be supplanted with a source-to-drain path, not to a gate but to a drain in Roohparvar, to somehow meet the

present claims. This form of combination or modification is not permitted absent some suggestion for doing so in either of the references.

For at least the foregoing reasons, Applicants believe independent claims 1 and 20, as well as claims dependent therefrom, are not anticipated by the cited art. Accordingly, Applicants respectfully request removal of this rejection.

### **Section 103 Rejection**

Claims 2, 8-17, 19, and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of Cuevas, U.S. Patent Nos. 6,297,103 to Ahn et al. (hereinafter "Ahn"); 5,999,447 to Naura et al. (hereinafter "Naura"); 5,812,477 to Casper et al. (hereinafter "Casper"); 6,617,914 to Kothandaraman (hereinafter "Kothandaraman"); and Roohparvar. As discussed above, the combination of Cuevas and Roohparvar do not meet the criteria for establishing a case of *prima facie* obviousness as to amended independent claim 20 (which incorporates the limitations of claim 22). In addition, in light of the amendments to independent claim 1 which incorporate allowable subject matter, it is believed that dependent claims 2, 8, and 9 are in condition for allowance. The remaining rejection of claims 10-17 and 19 is hereby traversed.

To establish a case of *prima facie* obviousness of a claimed invention, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Second, there must be a reasonable expectation of success. As stated in MPEP 2143.01, the fact that references can be hypothetically combined or modified is not sufficient to establish a *prima facie* case of obviousness. See *In re Mills*, 916 F.2d. 680 (Fed. Cir. 1990). Finally, the prior art references must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d. 981 (CCPA 1974); MPEP 2143.03. Specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d., 1382 (CCPA 1970). Using these standards, Applicants contend that the cited art fails to teach or suggest all features of independent claim 10, some distinctive features of which are set forth in more detail below.

The combination of Cuevas, Naura, Casper, and Kothandaraman does not teach or suggest a pair of programming transistors with source-to-drain paths coupled between inputs of a pair of cross-coupled transistors and a gate of a pair of selecting transistors. Present independent claim 10 makes clear that the programming transistors have a source-to-drain path that is coupled between inputs of a pair of cross-coupled transistors (which form a latch) and a gate of a pair of selecting transistors. This distinction was brought out above when traversing the rejection of independent claim 20. However, in addition to Cuevas and Roohparvar lacking any suggestion of the present claimed combination, the teachings of Naura, Casper, and Kothandaraman also lack any such suggestion. In fact, the Office Action admits on page 8 that the combination of Cuevas, Naura, Casper, and Kothandaraman "does not disclose a pair of programming transistors with source-to-drain paths coupled between the inputs of the pair of cross-coupled transistors and the gates of a pair of selecting transistors . . ." Instead, the Office Action alleges that Roohparvar fulfills the deficiencies of the failed combination. Applicant respectfully disagrees for the reasons discussed above when traversing the rejection of independent claim 20.

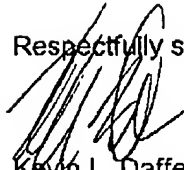
For at least the foregoing reasons, Applicants believe independent claims 1, 10, and 20, as well as claims dependent therefrom, are patentably distinct over the cited art. Accordingly, Applicants respectfully request removal of this rejection.

### **CONCLUSION**

The present amendment and response is believed to be a complete response to the issues raised in the Office Action mailed December 9, 2005. In view of the remarks traversing the rejections, Applicants assert that pending claims 1-6, 8-13, 15-21, and 23-25. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to Daffer McDaniel, LLP Deposit Account No. 50-3268/5298-18200.

Respectfully submitted,



Kevin L. Daffer  
Reg. No. 34,146  
Attorney for Applicant(s)

Daffer McDaniel, LLP  
P.O. Box 684908  
Austin, TX 78768-4908  
(512) 476-1400  
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